**OPT DESIGN:**

**Design Rule Check (DRC) Report**

**Design Name**: hello\_world\_arty\_a7

**Tool Version**: Vivado v.2018.3 (64-bit)

**Date**: October 17, 2024

**Host**: Samuel (64-bit)

**Device**: xc7a100ticsg324-1L

**Design State**: Synthesized

1. **Introduction**

This report documents the results of the Design Rule Check (DRC) performed on the synthesized design, "hello\_world\_arty\_a7," using the Xilinx Vivado tool version 2018.3. The DRC ensures that the design meets all the necessary design rules and is ready for further stages, such as implementation and deployment.

1. **Tool and Environment Overview** 
   * **Tool Version**: Vivado v.2018.3 (64-bit) o Build: 2405991 o Build Date: December 6, 2018
   * **Host System**: Samuel (64-bit operating system) o Build: 9200
   * **Command Executed**:

o report\_drc -file hello\_world\_arty\_a7\_drc\_opted.rpt -pb hello\_world\_arty\_a7\_drc\_opted.pb -rpx hello\_world\_arty\_a7\_drc\_opted.rpx

1. **Design Overview** 
   * **Design Name**: hello\_world\_arty\_a7
   * **Device**: xc7a100ticsg324-1L
   * **Design State**: Synthesized
   * **Speed Grade**: -1L
   * **Netlist**: netlist
   * **Floorplan**: design\_1
   * **Design Limits**: The entire design was considered.

1. **DRC Summary** 
   * **Ruledeck**: Default
   * **Max Violations Allowed**: Unlimited
   * **Violations Found**: 0 violations

The Design Rule Check (DRC) for the "hello\_world\_arty\_a7" design was executed with the default ruledeck, which enforces all relevant design rules for the selected device (xc7a100ticsg324-1L). The DRC found no violations in the design, indicating that it complies with all applicable design rules.

1. **Report Details**

There are no specific rule violations to report. The table below would typically summarize any issues, but since there were no violations, the table is empty.

|  |  |  |  |
| --- | --- | --- | --- |
| **Rule** | **Severity** | **Description** | **Violations** |
| - | - | - | 0 |

1. **Conclusion**

The DRC for the design "hello\_world\_arty\_a7" has successfully passed without any violations. This indicates that the design meets all the necessary design constraints and can proceed to the next stages of the design flow.

# Pinout Report

1. **Introduction**

This report presents the pinout details for an FPGA device, summarizing the available pins, their electrical range, I/O assignments, and other relevant attributes. The data presented is useful for hardware engineers working on PCB designs or system integrations involving this FPGA.

1. **Pinout Table**

The following table provides a detailed description of each pin, including its name, range, I/O assignment, electrical characteristics, and any special notes where applicable.

**Pinout Summary**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Pin Name | Range | Pin Function | I/O Assignment | Associated Bank | Notes |
| P1 | High Range | IO\_L6P\_T0\_D05\_14 | User I/O | Bank 14 | General purpose user I/O |
| P2 | High Range | IO\_L6N\_T0\_D04\_14 | User I/O | Bank 14 | General purpose user I/O |
| P3 | High Range | IO\_L3N\_T0\_DQS\_14 | User I/O | Bank 14 | Data strobe signal |
| P4 | High Range | IO\_L3P\_T0\_DQS\_14 | User I/O | Bank 14 | Data strobe signal |
| P5 | GND | GND | Ground | - | Ground pin |
| P6 | High Range | IO\_L1N\_T0\_AD0N\_14 | User I/O | Bank 14 | Analog/Digital signal pin |
| P7 | High Range | IO\_L1P\_T0\_AD0P\_14 | User I/O | Bank 14 | Analog/Digital signal pin |
| P8 | VCCO | Power | Bank 14 | VCCO |  |
| P9 | High Range | IO\_L24N\_T3\_A00\_D16\_14 | User I/O | Bank 14 | Data signal pin |
| P10 | High Range | IO\_L24P\_T3\_A01\_D17\_14 | User I/O | Bank 14 | Data signal pin |
| P11 | High Range | IO\_L25N\_T3\_DQS\_14 | User I/O | Bank 14 | Data strobe signal |
| P12 | High Range | IO\_L25P\_T3\_DQS\_14 | User I/O | Bank 14 | Data strobe signal |
| P13 | High Range | IO\_L26N\_T3\_A02\_D18\_14 | User I/O | Bank 14 | Data signal pin |
| P14 | GND | GND | Ground | - | Ground pin |
| P15 | High Range | IO\_L27P\_T3\_A03\_D19\_14 | User I/O | Bank 14 | Data signal pin |
| P16 | High Range | IO\_L27N\_T3\_A04\_D20\_14 | User I/O | Bank 14 | Data signal pin |
| P17 | High Range | IO\_L28P\_T3\_A05\_D21\_14 | User I/O | Bank 14 | Data signal pin |
| P18 | High Range | IO\_L9N\_T1\_DQS\_D13\_14 | User I/O | Bank 14 | Data strobe signal |
| R1 | High Range | IO\_L17P\_T2\_34 | User I/O | Bank 34 | General purpose user I/O |
| R2 | High Range | IO\_L15N\_T2\_DQS\_34 | User I/O | Bank 34 | Data strobe signal |
| R3 | High Range | IO\_L11P\_T1\_SRCC\_34 | User I/O | Bank 34 | Clock signal pin |
| R4 | GND | GND | Ground | - | Ground pin |
| R5 | High Range | IO\_L19N\_T3\_VREF\_34 | User I/O | Bank 34 | Voltage reference pin |
| R6 | High Range | IO\_L19P\_T3\_34 | User I/O | Bank 34 | General purpose user I/O |
| R7 | High Range | IO\_L23P\_T3\_34 | User I/O | Bank 34 | General purpose user I/O |
| R8 | High Range | IO\_L24P\_T3\_34 | User I/O | Bank 34 | General purpose user I/O |
| R9 | Dedicated | VCCO\_0 | VCCO | Bank 0 | Power supply for I/O banks |
| R10 | High Range | IO\_25\_14 | User I/O | Bank 14 | General purpose user I/O |
| R11 | High Range | IO\_0\_14 | User I/O | Bank 14 | General purpose user I/O |
| R12 | High Range | IO\_L5P\_T0\_D06\_14 | User I/O | Bank 14 | Data signal pin |
| R13 | GND | GND | Ground | - | Ground pin |
| R14 | High Range | IO\_L13N\_T2\_MRCC\_14 | User I/O | Bank 14 | Clock signal pin |
| R15 | High Range | IO\_L15P\_T2\_DQS\_RDWR\_B\_14 | User I/O | Bank 14 | Data strobe signal |
| R16 | High Range | IO\_L19N\_T3\_VREF\_34 | User I/O | Bank 34 | Voltage reference pin |
| R17 | High Range | IO\_L12N\_T1\_MRCC\_14 | User I/O | Bank 14 | Clock signal pin |
| R18 | High Range | IO\_L7P\_T1\_D09\_14 | User I/O | Bank 14 | Data signal pin |
| T1 | High Range | IO\_L17N\_T2\_34 | User I/O | Bank 34 | General purpose user I/O |
| T2 | High Range | VCCO\_34 | VCCO | Bank 34 | Power supply for I/O banks |
| T3 | High Range | IO\_L11N\_T1\_SRCC\_34 | User I/O | Bank 34 | Clock signal pin |
| T4 | High Range | IO\_L12N\_T1\_MRCC\_34 | User I/O | Bank 34 | Clock signal pin |
| T5 | High Range | IO\_L12P\_T1\_MRCC\_34 | User I/O | Bank 34 | Clock signal pin |
| T6 | High Range | IO\_L23N\_T3\_34 | User I/O | Bank 34 | General purpose user I/O |
| T7 | GND | GND | Ground | - | Ground pin |
| T8 | High Range | IO\_L24N\_T3\_34 | User I/O | Bank 34 | General purpose user I/O |
| T9 | High Range | IO\_L24P\_T3\_A01\_D17\_14 | User I/O | Bank 14 | Data signal pin |
| T10 | High Range | IO\_L24N\_T3\_A00\_D16\_14 | User I/O | Bank 14 | Data signal pin |
| T11 | High Range | IO\_L19P\_T3\_A10\_D26\_14 | User I/O | Bank 14 | Data signal pin |
| T12 | High Range | VCCO\_14 | VCCO | Bank 14 | Power supply for I/O banks |
| T13 | High Range | IO\_L23P\_T3\_A03\_D19\_14 | User I/O | Bank 14 | Data signal pin |
| T14 | High Range | IO\_L14P\_T2\_SRCC\_14 | User I/O | Bank 14 | Clock signal pin |
| T15 | High Range | IO\_L14N\_T2\_SRCC\_14 | User I/O | Bank 14 | Clock signal pin |
| T16 | High Range | IO\_L16P\_T2\_A07\_D23\_14 | User I/O | Bank 14 | Data signal pin |
| T17 | GND | GND | Ground | - | Ground pin |
| T18 | High Range | VCCO\_34 | VCCO | Bank 34 | Power supply for I/O banks |

1. **Special Considerations** 
   * **VCCO Requirements:** Some VCCO pins are marked with special requirements. These pins should be treated with care to ensure the proper functioning of the corresponding I/O bank.
   * **Ground (GND):** Pins marked as GND should be connected to the system

ground. These pins are critical for maintaining the device's electrical stability.

* + **Clock Signal Pins:** Certain pins are designated for clock signals (e.g., IO\_L11P\_T1\_SRCC\_34). It is essential to use these pins correctly in timingsensitive applications.
  + **Data Strobe (DQS) Pins:** Pins labelled as DQS are data strobe signals, used in certain memory and data bus interfaces for synchronizing data transfer.

## Conclusion

## This report provides an exhaustive view of the pin configuration for the FPGA device, offering guidance on how each pin should be used in a design. For more detailed electrical specifications, please refer to the device datasheet or family documentation. Proper assignment of I/O, power, and ground pins is essential for the stable and efficient operation of the FPGA in any embedded or hardware system.

# Vivado Bus Skew and DRC Report

**Tool Information**

* **Tool Version:** Vivado v.2018.3 (win64)
* **Build Date:** December 6, 2018
* **Date of Report:** October 17, 2024

**Host:** Samuel (64-bit major release)

* **Design:** hello\_world\_arty\_a7
* **Device:** xc7a100ti

1. **Bus Skew Report** 
   * **Bus Skew Constraints:** None specified
   * **Result:** No violations or issues found related to bus skew.

1. **DRC Report Summary** 
   * **Netlist:** netlist
   * **Floorplan:** design\_1
   * **Design Limits:** Entire design considered
   * **Ruledeck:** default
   * **Max Violations:** Unlimited
   * **Violations Found:** 0

**DRC Violations Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| **Rule** | **Severity** | **Description** | **Violations** |
| (none) | (none) | (none) | 0 |

## Vivado Methodology and Power Report Summary

**Tool Information**

* **Tool Version:** Vivado v.2018.3 (win64)
* **Build Date:** December 6, 2018
* **Date of Report:** October 17, 2024
* **Host:** Samuel (64-bit major release)
* **Design:** hello\_world\_arty\_a7
* **Device:** xc7a100ti

1. **Methodology Report Summary** 
   * **Netlist:** netlist

**Floorplan:** design\_1

* + **Design Limits:** Entire design considered
  + **Violations Found:** 2

**Violations Summary**

|  |  |  |  |
| --- | --- | --- | --- |
| **Rule** | **Severity** | **Description** | **Violations** |
| SYNTH-6 | Warning | Timing of a block RAM might be sub-optimal | 2 |

**Details of Violations**

* 1. **SYNTH-6#1**: The timing for rvsteel\_ram\_instance/ram\_reg\_0 might be suboptimal as no output register was merged into the block.
  2. **SYNTH-6#2**: The timing for rvsteel\_ram\_instance/ram\_reg\_1 might be suboptimal for the same reason.

**Design Route Status**

* + Total Logical Nets: 5418
  + Fully Routed Nets: 3877
  + Routing Errors: 0

1. **Power Report**

**Summary**

* + **Total On-Chip Power:** 0.080 W
  + **Dynamic Power:** 0.009 W
  + **Static Power:** 0.071 W
  + **Max Ambient Temperature:** 99.6 °C
  + **Junction Temperature:** 25.4 °C
  + **Confidence Level:** Medium

**On-Chip Components Power Consumption**

|  |  |  |  |
| --- | --- | --- | --- |
| **Component** | **Power (W)** | **Used** | **Utilization (%)** |
| Clocks | 0.003 | 4 | - |
| Slice Logic | 0.002 | 4916 | - |

|  |  |  |  |
| --- | --- | --- | --- |
| **Component** | **Power (W)** | **Used** | **Utilization (%)** |
| Block RAM | 0.002 | 2 | 1.48 |
| I/O | <0.001 | 3 | 1.43 |
| **Total** | **0.080** |  |  |

**Power Supply Summary**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Source** | **Voltage (V)** | **Total (A)** | **Dynamic (A)** | **Static (A)** |
| Vccint | 0.950 | 0.019 | 0.010 | 0.009 |
| Vccaux | 1.800 | 0.016 | 0.000 | 0.016 |
| Vccadc | 1.800 | 0.018 | 0.000 | 0.018 |

1. **Confidence Level** 
   * **Design Implementation State:** High (Design is routed)
   * **Clock Nodes Activity:** High (More than 95% of clocks specified)
   * **I/O Nodes Activity:** Medium (Missing specification for >5% of inputs)
   * **Internal Nodes Activity:** Medium (Specified for <25% of internal nodes)
   * **Overall Confidence Level:** Medium

**Conclusion**

The design **hello\_world\_arty\_a7** has some warnings related to block RAM timing, which might affect performance. However, the power consumption is low, and the overall design state is acceptable with no routing errors.

## Implementation Report

**Project Overview**

**Project Name:** Hello World

**Target Device:** XC7A100T-1CSG324

**Location:** C:/Users/sabolu samuel jason/riscv-gnutoolchain/riscvsteel/examples/hello\_world/boards/arty\_a7/ **Implementation Phases**

1. **Synthesis Phase** 
   * + **Start Time:** 00:00:00
     + **End Time:** 00:00:05
     + **Elapsed Time:** 5 seconds
     + **Peak Memory Usage:** 1493.020 MB
     + **Warnings:** 0
     + **Errors:** 0
2. **Placement Phase** 
   1. **Pipeline Register Optimization**  **Elapsed Time:** 7 seconds
      * **Peak Memory Usage:** 1493.020 MB
   2. **Post Placement Optimization**  **Elapsed Time:** 10 seconds  **Peak Memory Usage:** 1493.020 MB
      * **Post Placement Timing Summary:** o **WNS:** 0.652
3. **Routing Phase** 
   * + **Start Time:** 00:00:20
     + **End Time:** 00:00:44
     + **Elapsed Time:** 24 seconds
     + **Peak Memory Usage:** 1592.492 MB
   1. **Routing Initialization** 
      * **Elapsed Time:** 20 seconds
      * **Nodes with overlaps:** o Initial: 2219 o Final: 0
      * **Intermediate Timing Summary:**
        + **WNS:** 0.512
        + **TNS:** 0.000
4. **Post Routing Analysis** 
   * + **DRC Report Location:** C:/Users/sabolu samuel jason/riscv-gnutoolchain/riscvsteel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7

\_100t/runs/impl\_1/hello\_world\_arty\_a7\_drc\_routed.rpt

* + - **Methodology Report Location:** C:/Users/sabolu samuel jason/riscv-gnutoolchain/riscvsteel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7

\_100t/runs/impl\_1/hello\_world\_arty\_a7\_methodology\_drc\_routed.rpt

* + - **Power Report Location:** C:/Users/sabolu samuel jason/riscv-gnutoolchain/riscvsteel/examples/hello\_world/boards/arty\_a7/hello\_world\_arty\_a7

\_100t/runs/impl\_1/hello\_world\_arty\_a7\_power\_routed.rpt **Summary of Results**

* + - **Total Implementation Time:** 44 seconds
    - **Total Warnings:** 0
    - **Total Errors:** 0
    - **Final Timing Summary:** o **WNS:** 0.512 o **TNS:** 0.000

**Conclusion**

The design implementation for the Hello World project targeting the XC7A100T1CSG324 FPGA was completed successfully without any warnings or errors. The timing analysis indicates that the design meets the required specifications, with the worst negative slack (WNS) being positive.

## FPGA Utilization Report

**Tool Version:** Vivado v.2018.3

**Design:** hello\_world\_arty\_a7

**Device:** 7a100ticsg324-1L

**Design State:** Fully Placed

**Date:** Thu Oct 17 09:48:08 2024

**Host:** Samuel running 64-bit major release (build 9200)

1. **Slice Logic**

**Summary of Utilization**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **Slice LUTs** | 2394 | 63400 | 3.78 |
| **Slice Registers** | 1768 | 126800 | 1.39 |
| **F7 Muxes** | 339 | 31700 | 1.07 |
| **F8 Muxes** | 0 | 15850 | 0.00 |

**Summary of Registers by Type**

|  |  |  |  |
| --- | --- | --- | --- |
| **Total Registers** | **Clock Enable** | **Synchronous** | **Asynchronous** |
| 0 | - | - | - |
| 0 | - | - | Set |
| 0 | - | - | Reset |
| 0 | Yes | - | - |
| 88 | Yes | Set | - |
| **Total Registers** | **Clock Enable** | **Synchronous** | **Asynchronous** |
| 1680 | Yes | Reset | - |

1. **Slice Logic Distribution**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | **Site Type** | | **Slice** | | **LUT as Logic** | | **Slice Registers** | | **Unique Control Sets** | | |  | | --- | | **Used** | | 843 | | 2394 | | 1768 | | 62 | | |  | | --- | | **Available** | | 15850 | | 63400 | | 126800 | | 15850 | | |  | | --- | | **Util%** | | 5.32 | | 3.78 | | 1.39 | | 0.39 | |

1. **Memory**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **Block RAM Tile** | 2 | 135 | 1.48 |

1. **DSP**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **DSPs** | 0 | 240 | 0.00 |

1. **I/O and GT Specific**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **Bonded IOB** | 3 | 210 | 1.43 |

1. **Clocking**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **BUFGCTRL** | 2 | 32 | 6.25 |

1. **Specific Feature**

|  |  |  |  |
| --- | --- | --- | --- |
| **Site Type** | **Used** | **Available** | **Util%** |
| **BSCANE2** | 0 | 4 | 0.00 |

1. **Primitives**

|  |  |  |
| --- | --- | --- |
| **Ref Name** | **Used** | **Functional Category** |
| **FDRE** | 1680 | Flop & Latch |
| **LUT6** | 1270 | LUT |
| **MUXF7** | 339 | MuxFx |
| **RAMB36E1** | 2 | Block Memory |

1. **Black Boxes**

|  |  |
| --- | --- |
| **Ref Name** | **Used** |
| - | 0 |

1. **Instantiated Netlists**

|  |  |
| --- | --- |
| **Ref Name** | **Used** |
| - | 0 |

**Conclusion**

The FPGA design demonstrates efficient utilization, with most resources well below their limits. This indicates that there is significant room for expansion or optimization in your design. You may also consider evaluating the usage of DSPs and Block RAM, as their utilization is currently low.

## Vivado Control Set Report

**Tool Information**

* **Tool Version:** Vivado v.2018.3 (win64)
* **Build Date:** December 6, 2018
* **Date of Report:** October 17, 2024
* **Host:** Samuel (64-bit major release)
* **Design:** hello\_world\_arty\_a7
* **Device:** xc7a100ti

1. **Summary** 
   * **Number of Unique Control Sets:** 62
   * **Unused Register Locations in Slices Containing Registers:** 72

1. **Histogram of Control Sets by Fanout**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | **Fanout** | | 1 | | 4 | | 5 | | 6 | | 8 | | 9 | | 13 | | 14 | | **16+** | | |  | | --- | | **Control Sets** | | 1 | | 3 | | 2 | | 1 | | 3 | | 2 | | 1 | | 1 | | **48** | |

1. **Flip-Flop Distribution**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Clock Enable** | **Synchronous Set/Reset** | **Asynchronous Set/Reset** | **Total**  **Registers** | **Total Slices** |
| No | No | No | 23 | 16 |
| No | No | Yes | 0 | 0 |
| No | Yes | No | 188 | 70 |
| Yes | No | No | 9 | 5 |
| Yes | No | Yes | 0 | 0 |
| Yes | Yes | No | 1548 | 565 |

1. **Detailed Control Set Information**

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | **Clock Signal** | | |  |  |  |  | | --- | --- | --- | --- | | **Enable Signal** | **Set/Reset Signal** | **Sli ce**  **Lo**  **ad**  **C ou nt** | **Be**  **l**  **Lo**  **ad**  **Co un**  **t** | | | | |
| |  | | --- | | clock\_IB  UF\_BUF  G | | clock\_50 mhz\_BU FG | | clock\_50 mhz\_BU FG | | clock\_50 mhz\_BU FG | | |  | | --- | |  | | rvsteel\_mcu\_instance/rvsteel\_co re\_instance/current\_state[3]\_i\_2 \_n\_0 | |  | | rvsteel\_mcu\_instance/rvsteel\_sp i\_instance/bit\_count[3]\_i\_2\_n\_0 | | |  | | --- | |  | | rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 | | rvsteel\_mcu\_instance/rvsteel\_s pi\_instance/curr\_state0 | | rvsteel\_mcu\_instance/rvsteel\_s pi\_instance/cycle\_counter1 | | |  | | --- | | 1 | | 1 | | 3 | | 1 | | |  | | --- | | 1 | | 4 | | 4 | | 4 | |

|  |
| --- |
| **t** |

|  |
| --- |
| **nt** |

|  |
| --- |
| 5 |
| 5 |
| 6 |
| 8 |
| 8 |
| 8 |
| 9 |
| 9 |
| 13 |

|  |
| --- |
| 5 |
| 3 |
| 6 |
| 2 |
| 2 |
| 3 |
| 3 |
| 5 |
| 4 |

|  |
| --- |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/prev\_write\_reques t\_reg\_1[0] |
| rvsteel\_mcu\_instance/rvsteel\_u art\_instance/reset\_internal |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_s pi\_instance/cycle\_counter[7]\_i\_  1\_n\_0 |
| reset\_debounced |
| reset\_debounced |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/SR[0] |
|  |
| rvsteel\_mcu\_instance/rvsteel\_u art\_instance/tx\_register |

|  |
| --- |
|  |
|  |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mcause[31]\_i\_1 \_n\_0 |
|  |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/mtimecmp[31]\_i\_2\_  0[0] |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/prev\_rw\_address\_re g[3]\_0[0] |
|  |
| rvsteel\_mcu\_instance/rvsteel\_ua rt\_instance/tx\_register |
|  |

|  |
| --- |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |

clock\_50

|  |
| --- |
| **t** |

|  |
| --- |
| **nt** |

|  |
| --- |
| 14 |
| 19 |
| 22 |
| 26 |
| 30 |
| 31 |
| 31 |
| 32 |
| 32 |

|  |
| --- |
| 7 |
| 7 |
| 15 |
| 18 |
| 8 |
| 15 |
| 18 |
| 8 |
| 13 |

|  |
| --- |
| reset\_debounced |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
|  |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/csr\_mcause[30]\_i\_  1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_u art\_instance/rx\_cycle\_counter[0] \_i\_1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |

|  |
| --- |
|  |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mie\_mfie0 |
|  |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mcause[31]\_i\_1 \_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mepc[31]\_i\_1\_n \_0 |
| rvsteel\_mcu\_instance/rvsteel\_bu s\_instance/E[0] |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mtvec1 |
|  |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[15][31]\_i \_1\_n\_0 |

|  |
| --- |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |

clock\_50

|  |
| --- |
| **t** |

|  |
| --- |
| **nt** |

|  |
| --- |
| 32 |
| 32 |
| 32 |
| 32 |
| 32 |
| 32 |
| 32 |
| 32 |
| 32 |

|  |
| --- |
| 8 |
| 19 |
| 11 |
| 8 |
| 19 |
| 9 |
| 14 |
| 12 |
| 12 |

|  |
| --- |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |
| rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 |

|  |
| --- |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_minstret[31]\_i\_1 \_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mtval[31]\_i\_1\_n \_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[23][31]\_i \_1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_minstret[63]\_i\_1 \_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/csr\_mscratch0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[3][31]\_i\_  1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[21][31]\_i \_1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[11][31]\_i \_1\_n\_0 |
| rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[17][31]\_i \_1\_n\_0 |

|  |
| --- |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |
| clock\_50 mhz\_BU FG |

clock\_50

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  | | --- | | **Clock Signal** | | |  | | --- | | **Enable Signal** | | |  | | --- | | **Set/Reset Signal** | | |  | | --- | | **ad C ou nt** | | |  | | --- | | **ad**  **Co un**  **t** | | |
| clock\_50 mhz\_BU FG | rvsteel\_mcu\_instance/rvsteel\_co re\_instance/integer\_file[10][31]\_i \_1\_n\_0 | rvsteel\_mcu\_instance/rvsteel\_c ore\_instance/reset\_internal\_1 | 9 | 32 |

1. **Conclusion**

This report provides a comprehensive overview of the control set information for the hello\_world\_arty\_a7 design. The detailed analysis of control sets by fanout, flip-flop distribution, and clock, enable, and reset signals can help in further optimization and design validation processes.